ANSI/VITA 10-1995 (R2002)

American National Standard
for SKYchannel Packet Bus on VME P2

Secretariat
VMEbus International Trade Association

Approved 1995, Reaffirmed 2002
American National Standards Institute, Inc.

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Abstract
This standard provides a specification of the data link protocol and physical interface of a high performance packet bus extension to the VME standard. This extension consists of high bandwidth, low latency packet bus transfers between VMEbus modules using the P2 connector and a network of crossbar designs..

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1 Introduction

SKYchannel is a 320 MB/sec Packet Bus architecture developed by SKY Computers Inc. This architecture provides high throughput, scalable I/O and processing to support applications that range from single board solutions to solutions with multiple processors on multiple boards in multiple chassis.

To achieve high performance data transfers, multiple VME boards are connected together using SKYchannel Backplanes. SKYchannel Backplanes are active backplane daughtercards that plug onto the P2 connector of the VME chassis using rows A and C for signals. The SKYchannel also uses two pins on Row B for power and two pins for ground. Multiple SKYchannel Backplanes may be linked together to connect multiple clusters of boards, possibly in multiple chassis, into a single SKYchannel system.

FIFOs and packet controllers at each SKYchannel interface ensure that packets are built continuously and data pipelines are filled. The SKYchannel architecture is designed to support multiple implementations. An example of one implementation is point-to-point interconnects with crossbars for maximum bandwidth, and multidrop bus backplanes for low-cost and minimum power consumption. Another is a bussed implementation that would provide a single SKYchannel data path that can be accessed by multiple boards. The bus implementation offers a lower cost, lower power alternative for applications requiring only a single data path. For higher speed applications, the crossbar switch implementation provides multiple simultaneous high-speed SKYchannel data paths to minimize processor blocking and maximize bisectional bandwidth for optimal multiprocessor performance. An example crossbar implementation with 10 ports and five simultaneous 320 MB/sec paths per level provides an aggregate data bandwidth of 1600 MB/sec. Figure 1 shows the physical connections of a SKYchannel enabled VME board and SKYchannel Backplane (the standard VME backplane is not shown).

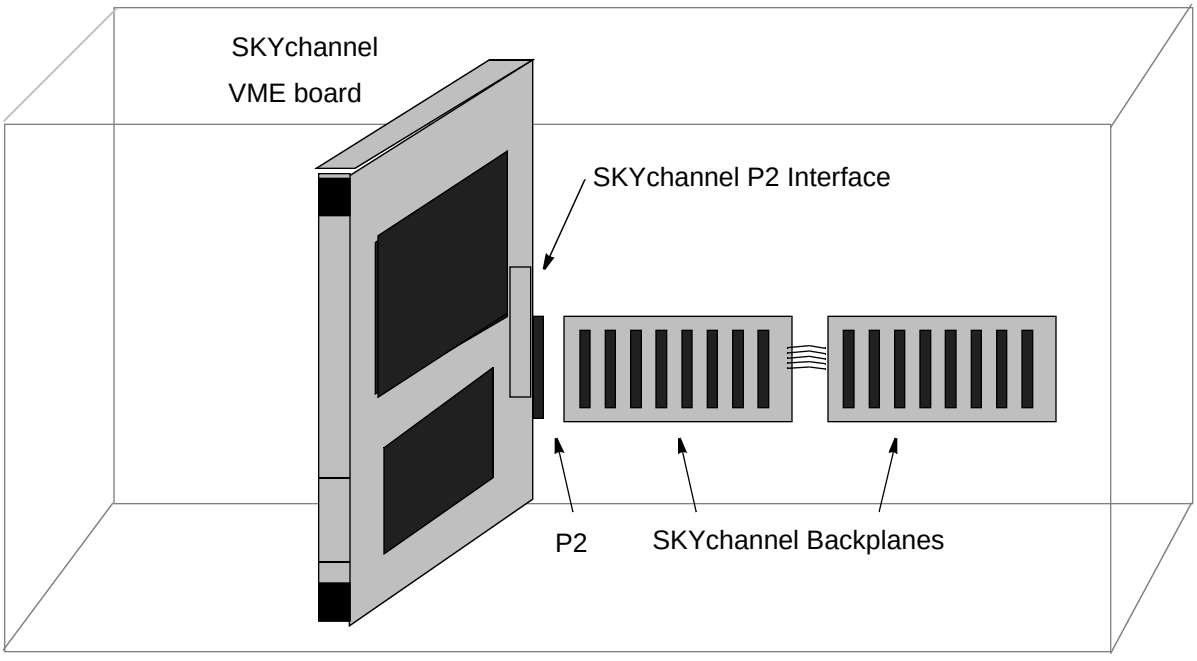


Figure 1 - SKYchannel Extender and SKYchannel Backplanes

Figure 2 shows an example of a bus backplane utilizing a single SKYchannel data path.

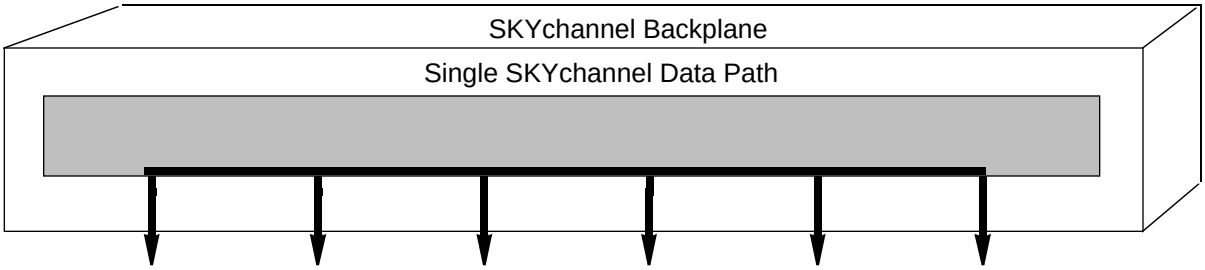


Figure 2 - SKYchannel Backplane: Example Bus Implementation

Figure 3 shows how five ports can transmit simultaneously with the crossbar implementation. The switching and arbitration occurs in hardware to eliminate software overhead for setup and data routing.

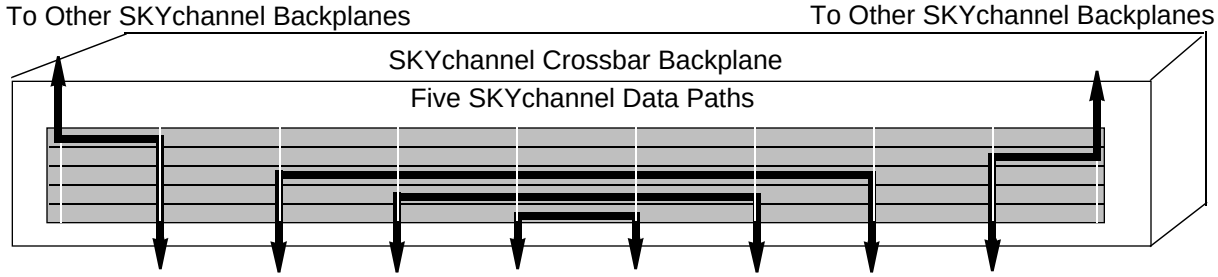


Figure 3 - SKYchannel Backplane: Example Crossbar Implementation

The SKYchannel Packet Bus features are supported between VME boards, VME chassis, and VME systems. The SKYchannel Protocol supports 16 Terabytes of global addressing and systems with up to 256 boards. Figure 4 shows a system with multiple SKYchannels connected in a daisy chain configuration. Note that the physical layer of this standard does not cover the implementation of the connections internal to the SKYchannel Backplane or the connections between backplanes.

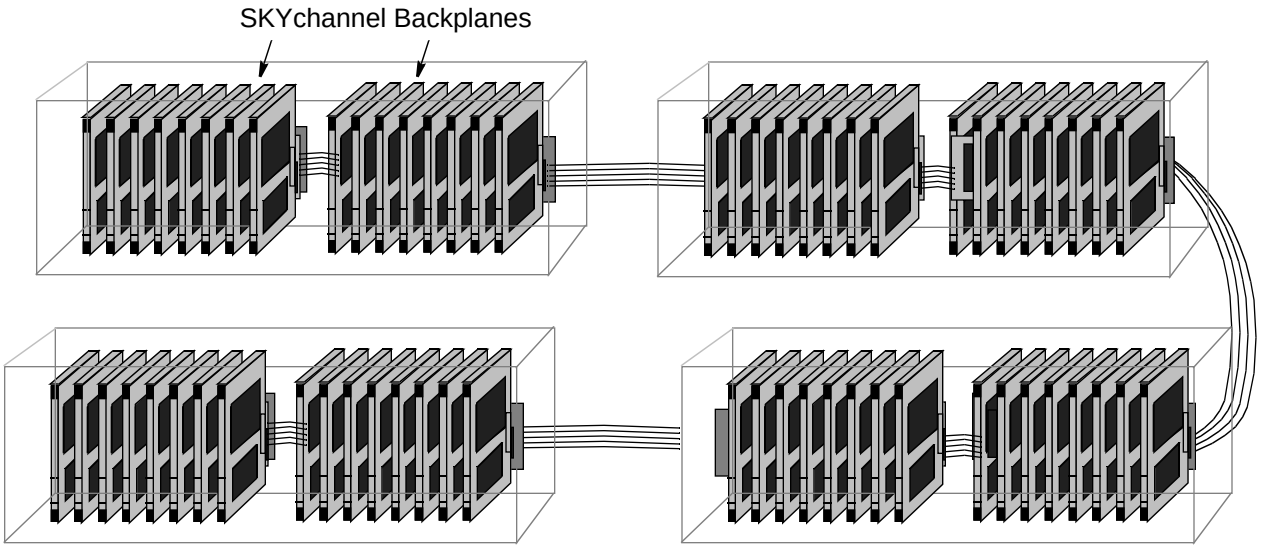


Figure 4 - Example of Multiple SKYchannels in a Daisy Chain Configuration

It is also possible to design systems with multiple SKYchannel busses or crossbars in a hierarchical configuration. An example using 10-port crossbars is diagrammed in Figure 5-

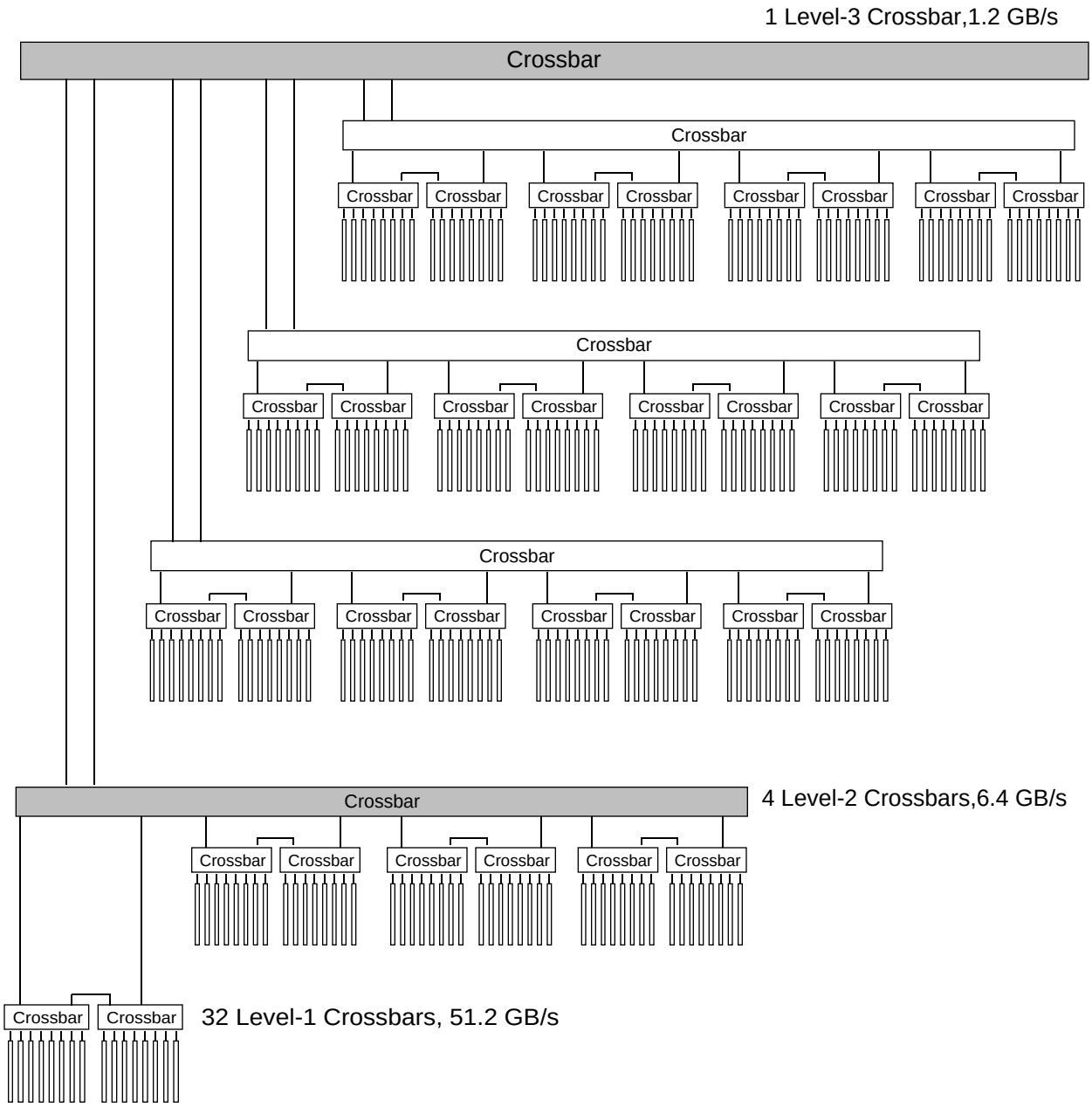


Figure 5 - Example of Multiple SKYchannels in a Hierarchical Configuration

2 Scope and Purpose

2.1 Scope

This standard describes a high performance SKYchannel Packet Bus architecture that is fully compatible with the VMEbus standards ([1], [2]). This standard addresses communication between VME boards using the P2 connector. This includes the physical layer for communication between the VME board and a SKYchannel Backplane through VME P2/J2, and the data link layer for communication from board to board. This standard does not address the physical layer for running SKYchannel within a SKYchannel Backplane or group of Backplanes, which is considered an implementation detail. The standard includes specifics of the packet protocol, signals, waveforms, timing diagrams and mechanical specifications.

2.2 Purpose

The purpose of this specification is to provide information needed to design VMEbus boards that can interface with the SKYchannel Packet Bus architecture.

2.3 References

[1] ANSI/IEEE STD 1014-1987, VMEbus Specification.

[2] ANSI/VITA 1-1994, VME64 Specification

[3] ISO 7498, Open Systems Interconnection (OSI) Reference Model, Oct, 1984.

[4] ANSI/IEEE STD 1101.1-1991, IEEE Standard for Mechanical Core Specifications for Microcomputers.

3 Definitions

The following are definitions of terms used in this specification:

3.1 Key Words

Shall: A key word indicating a requirement. Requirements must be met to conform to the standard.

Should: A key word indicating an option with a preferred or recommended implementation.

May: A key word indicating an option with no specific preference.

3.2 General

Data Link Layer: The Open Systems Interconnection (OSI) reference model [3] layer specifying the low level logical protocol.

Physical Layer: The OSI reference model layer specifying electrical and mechanical specifications.

3.3 Protocol

Multi-mastering: All the interfaces are capable of initiating and receiving transfers.

SKYchannel Protocol: The split transaction packet bus protocol that includes the Data Link Layer for SKYchannel.

SKYchannel Packet: The basic unit of communication containing both the address information and the data. The four SKYchannel packet types (write, interrupt, read, and compare & switch) handle all the functions required for a high-performance multiprocessor system.

Response packet: A write packet that is sent in response to a read packet.

Pword: A 72-bit quantity from which packets are composed. There are address, data, and checkword Pwords. An address Pword contains information needed for automatic packet routing and transparent addressing. A data Pword contains 64 bits of data and 8 bits of enable and control information. A checkword is 72 parity bits.

3.4 Physical

SKYchannel P2 Interface: Control logic on a VME board that provides the interface between the local on-board bus and the SKYchannel Backplane attached to VME J2.

SKYchannel Backplane: The backplane overlay daughterboard that plugs onto the rear VME J2 backplane connectors via DIN connectors.

Gbus: The electrical interface between the SKYchannel P2 Interface and the SKYchannel Backplane.

SKYchannel Architecture: The collection of the SKYchannel P2 Interface and SKYchannel Backplane running the SKYchannel protocol over the Gbus.

SKYchannel Backplane Controller: The lowest-numbered board connected to a particular SKYchannel Backplane. This board is responsible for handling interrupts generated on that Backplane.

RSV: Indicates reserved bits in address or data Pwords that shall always be driven low.

Master FIFO: A bidirectional FIFO that initiates read, write, compare & switch, and interrupt packets and receives response packets. A Master FIFO is required for the device to be able to initiate SKYchannel requests.

Slave FIFO: A bidirectional FIFO that initiates response packets and receives read, write, compare & switch and interrupt packets. A Slave FIFO is required for the device to be able to respond to SKYchannel requests.

Read FIFO: A portion of the Master and Slave FIFOs that transfers data from the SKYchannel Backplane.

Write FIFO: A portion of the Master and Slave FIFOs that transfers data to the SKYchannel Backplane.

Early Packet Available: The capability of a SKYchannel interface to begin forwarding a SKYchannel packet before the entire packet has been received in the FIFO of that SKYchannel interface. See Section 6.1.5 for a complete description of the use of the Packet Available (PA_) signal.

4 Overview

4.1 Characteristics

4.1.1 VMEbus Compatibility

The SKYchannel Backplane is compatible with the VMEbus and any VME extension not using rows A and C of the VME P2 connector. It coexists with VMEbus operations, requiring no VMEbus signals or extra slots.

4.1.2 Interconnectivity

The SKYchannel provides full interconnectivity through the SKYchannel Backplane; any processor can directly read or write data from/to any other devices connected to the SKYchannel Backplane. The SKYchannel protocol can directly address up to 256 boards in a single system.

4.1.3 Latency

The SKYchannel packet bus protocol is optimized for high-performance multi-processor communication. As shown in the timing diagrams, sending data takes as little as 4 cycles (100 nsec at 40 MHz) from assertion of the Packet Available (PA) signal at the initiator until the first data is available at the receiver. Once the first data word is received, 8 bytes can be transferred every clock cycle (25ns) for a 320 MB/sec maximum data rate per channel, with a maximum of 100ns latency to arbitrate for an available path when there is no contention for the path.

4.1.4 Transactions

The SKYchannel protocol supports four types of transactions:

- Basic Read Transaction
  Request data from SKYchannel address space.
- Basic Write Transaction
  Send data to SKYchannel address space.
- Compare and Switch Transaction
  Perform locked atomic access across the SKYchannel, e.g., for semaphore operations.
- Interrupt Transaction
  Issue an interrupt to a processor which resides on the SKYchannel.

SKYchannel supports Interprocessor Communication by allowing an unlimited number of mailbox registers in memory for semaphores. The SKYchannel hardware-implemented compare & switch operation allows fast access to semaphores.

4.1.5 Transaction Size

SKYchannel packets can be 3 to 131 Pwords long (1 to 129 data Pwords plus the address Pword and the checkword Pword). The SKYchannel architecture is designed to provide efficient data transfers that approach the maximum transfer rate even for packet sizes much less than the maximum. The effective transfer rate of SKYchannel is shown in Figure 12.

size := 1.129

oh := 4

$$xr := \frac{size}{oh + size} * 320\ MB/sec^{\dagger}$$

† Assumes 40MHz clock. If clock rate is reduced, transfer rate also decreases.

size = Transfer size in SKYchannel Data Pwords
oh = Overhead (see Table 5)
xr = Transfer rate

Figure 6 - SKYchannel Transfer Rate Calculation

4.2 Fundamental Concepts

4.2.1 Bus Interfaces

The SKYchannel bus architecture uses a standard interface to connect all functional SKYchannel interfaces on the SKYchannel bus. The SKYchannel interface includes a packet controller and one or more FIFOs. A full implementation of a SKYchannel interface supports four types of transfers: Master writes, Master reads, Slave writes, and Slave reads. Any given interface need only implement the appropriate subset of these transfers, but separate FIFOs are required for each transfer type implemented. Section 6.1.2 describes these requirements in detail. Transactions are routed automatically through these interfaces based on information contained in the packet headers. All data movement is buffered and pipelined so that a packet controller can continue to build new packets while the previous packet is transmitting. A SKYchannel interface may include a DMA controller.

4.2.2 Early Packet Available

The FIFO design does not require the packet to finish loading before starting the transfer; the transfer can start immediately. This capability is called *early packet available*, and is implemented in the Physical Layer as described in Section 6.1.5. On the surface, early packet available appears similar to the well-known networking concept of worm-hole routing. However, there are fundamental differences. The most important difference involves the treatment of sub-packets. In a worm-hole routed network sub-packets from different packets, called flits, may be interspersed. Such a relaxed protocol can create complications during packet assembly at the receiving interface. SKYchannel requires all packet sub-units, called Pwords, to be sent sequentially and without interspersing them with Pwords from other packets, thus avoiding such complications.

4.2.3 Routing

The logic on the SKYchannel Backplane reviews the address and automatically routes the packet to the destination address without interprocessor handshaking or tying up the bus through the entire network. The sender does not need to know the connection topology or any other routing information, providing maximum transparency and portability.

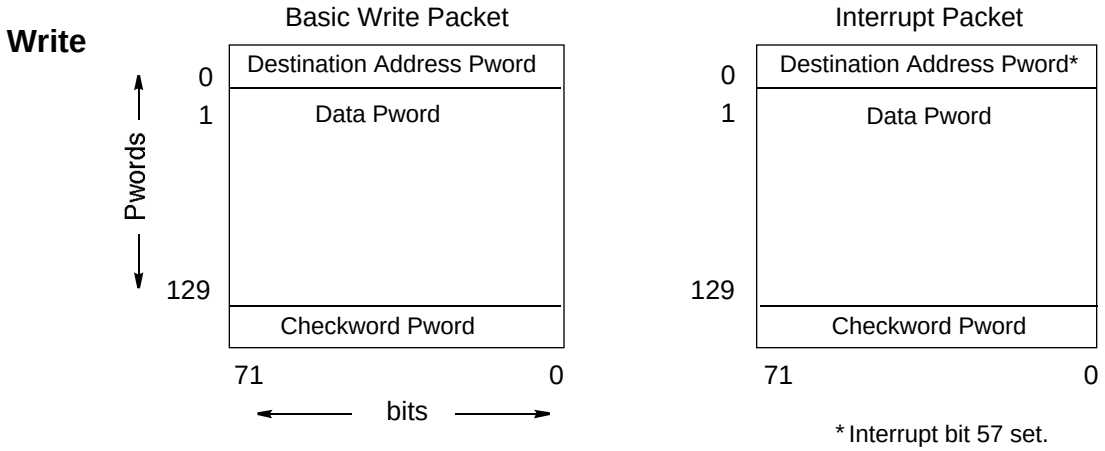
4.2.4 Packet Transfers and the SKYchannel Backplane

The SKYchannel P2 Interface attached to a SKYchannel Backplane port determines the packet's destination based on the contents of the SKYchannel address word. The SKYchannel Backplane determines which board is targeted, based on the contents of the address Pword.

5 Data Link Layer

5.1 Transaction Format

The information contained in the four types of SKYchannel packets (two write and two read) automatically routes data to the SKYchannel destination. Functionality such as interrupt, and atomic operation is built into the various SKYchannel packets. Packets are composed of three type of Pwords (address, data, and checkword). A checkword Pword at the end of each packet provides for error detection. The SKYchannel packets are diagrammed in Figure 7 and Figure 8.



Note: A data Pword contains four 16-bit data words

Figure 7 - SKYchannel Write Packets

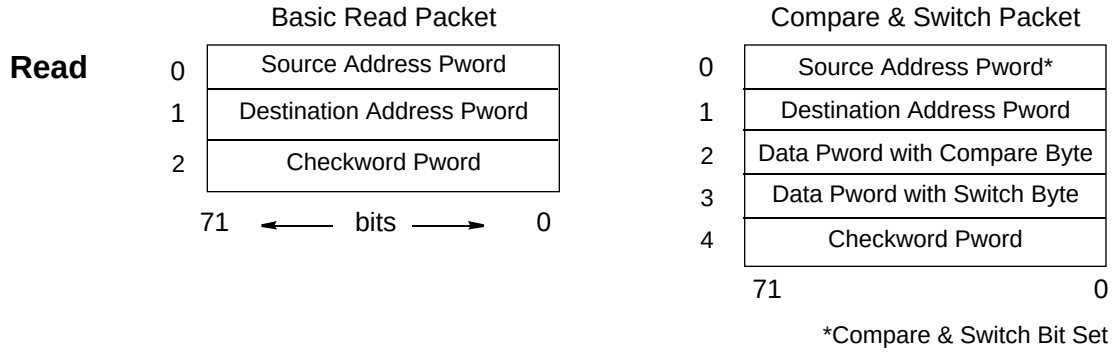


Figure 8 - SKYchannel Read Packets

5.1.1 Basic Write Packet

The Basic Write Packet shall consist of an address Pword, containing the destination address, followed by 1 to 129 data Pwords, followed by a checkword Pword. The address Pword shall have the WRT bit set. The destination address shall be 64-bit aligned. Note that an unaligned transfer can be accomplished by using the Byte Enable field in the data Pwords. The last data Pword shall have the EOP bit set. The maximum transfer size shall be 1024 bytes which may be unaligned with respect to the 64-bit address boundary. Note that the maximum transfer size of 129 data Pwords may result only during an unaligned transfer of more than 1016 bytes.

5.1.2 Basic Read Packet

The Basic Read Packet shall consist of three Pwords: two address Pwords followed by a checkword Pword. The first address Pword shall have the WRT bit cleared, indicating this not a write packet but a read packet. The first address Pword shall contain the source address and the number of 16-bit data words to be read. Although address Pwords are generally required to be 64-bit aligned (see Section 5.2), the source address Pword in a basic read packet may be 16-bit aligned. This enables only the exact set of 16-bit data words to be read from the data source.

The second Pword shall contain the destination address. This destination address should be an address serviced by the same SKYchannel P2 interface that generates the read packet. If the destination address Pword does contain an address serviced by the same SKYchannel P2 interface that generates the basic read packet, then the destination address Pword shall have the response packet bit (bit 65) set. The destination address shall be 64-bit aligned. Note that the byte enable field in data Pwords that are returned can facilitate writing an exact set of 16-bit data words (see section 5.3.3).

Upon receiving a basic read packet, a SKYchannel interface shall generate a basic write packet, in this case called a response packet, which returns the requested data. The destination address Pword from the read packet shall be used without modification as the destination Pword for the response packet. The data Pwords in this response packet shall contain the number of 16-bit data words requested in the basic read packet. The data words shall be 64-bit aligned, and the byte enable fields shall be set based on the 16-bit aligned source address in the read packet and the number of 16-bit data words requested.

5.1.3 Compare & Switch Packet

The Compare & Switch Packet is an extended form of the read packet. The compare & switch packet provides an atomic operation for functions such as semaphores and for positionless interprocess communication (IPC). When the destination interface sees a Compare & Switch packet, its hardware checks the appropriate memory location then changes the data immediately if the compare was equal. This is automatic and it requires no processor involvement. Because SKYchannel is a packet bus, atomic operations do not need to lock the circuit or the bus as would a circuit switch implementation.

The Compare & Switch packet shall consist of two address Pwords, followed by two data Pwords, followed by a checkword Pword. The first address Pword shall contain the 64-bit aligned source address, in this case the address to read for the comparison. This first address Pword shall have the CMS (compare & switch) bit set and the WRT bit cleared. The second address Pword shall contain the 64-bit aligned destination address, in this case where the result of the operation should be sent. This address shall be a valid location at the SKYchannel interface sending the Compare & Switch packet. The first data Pword is the compare Pword, while the second data Pword is the switch Pword. The compare Pword shall contains the compare byte in bits [0:7], which shall be replicated in bits [32:39]. This replication helps alleviate any endian issues. The second data Pword shall have the EOP bit set.

A SKYchannel P2 interface receiving a packet shall examine the CMS bit in the first Pword to determine whether it is a compare & switch cycle. The compare byte within the compare data Pword shall be compared against the data at the memory location addressed by the source address Pword. If this 8-bit comparison determines the compare byte is equal to the data currently in this memory location, the entire switch Pword shall be written into this memory location. If the compare fails then the switch word shall be ignored.

Once the Compare & Switch operation is complete, the interface shall return the result in the form of a write packet. This response packet shall consist of an address Pword, followed by a data Pword, followed by a

checkword Pword. The destination address Pword from the Compare & Switch packet shall be used as the address Pword. The 1-bit result of the Compare & Switch operation shall be placed in bit 0 of the data Pword and replicated in bit 32. The remaining bits are undefined. If the compare succeeds, the result shall be 0. If the compare fails, the result shall be 1. Note that no special operations need to be performed by the SKYchannel controller for compare & switch accesses.

5.1.4 Interrupt Packet

The Interrupt packet is a special form of a write packet. An interrupt packet shall have the interrupt (INT) bit set [57 = 1] in the address Pword. The Packet Specific Code (PSC) field [57:48] of address Pword shall be interpreted as interrupt mask bits. The meaning of these interrupt mask bits is defined by the implementation, and is expected to vary by functionality available on the boards containing a SKYchannel P2 interface. Boards that contain one or more processors should provide the capability to interrupt a particular processor based on the contents of the interrupt mask bits. The data that is sent with the packet shall be placed in memory at the address specified in the packet header word. This allows a message to be sent with the interrupt.

5.2 Address Pwords

The address Pword contains the routing and packet header information. The controllers on the interfaces use the bits in the address Pword to:

- Control routing.
- Indicate the packet type: read, write, compare & switch, or interrupt.
- Indicate the type of Pword, address or data.
- Indicate the End of Packet.

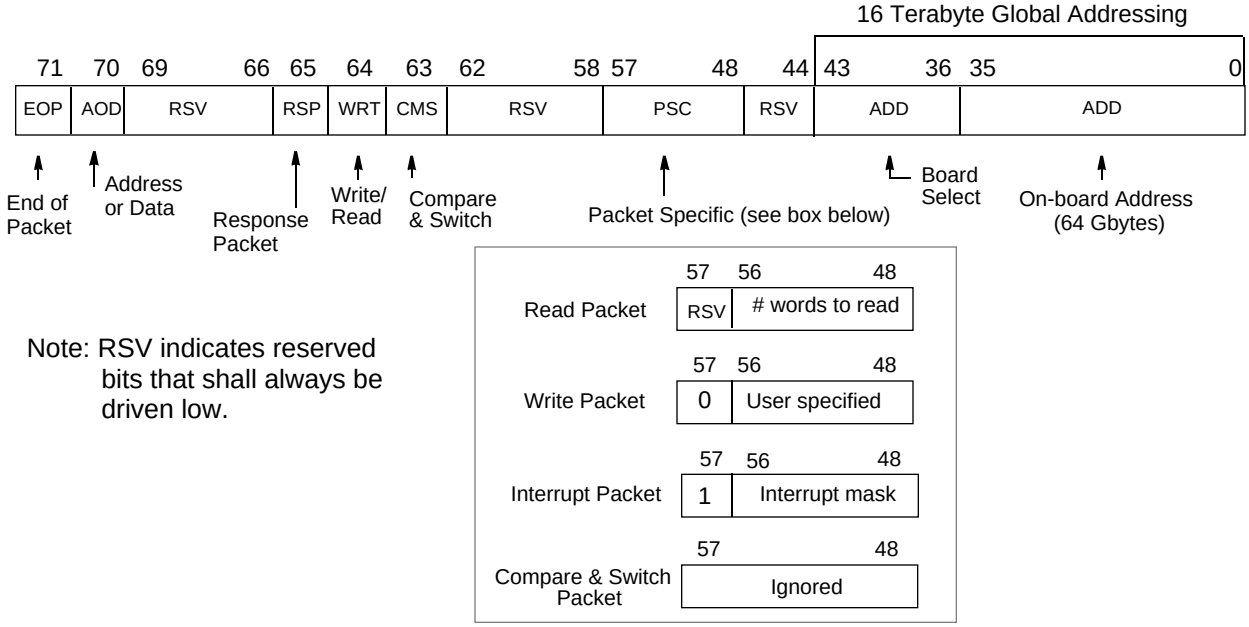
The address Pword contains the 44-bit, 16 Terabyte address in the lower order bits. The first 36 bits provide the capability for each SKYchannel board to contain up to 64 GBytes of local memory. All Pword addresses shall 64-bit aligned, with the exception of the source address Pword in a Basic Read Packet which shall be 16-bit aligned. The address Pword (shown in Figure 9) contains the information needed for automatic packet routing and transparent addressing.

5.2.1 End of Packet

The end of packet (EOP) bit shall be cleared [71=0] in the address Pword for all packets except the Read packet where the second Pword (destination address) is the last word of the read packet before the checkword.

5.2.2 Address or Data

The address or data (AOD) bit shall be cleared [70=0] in the address Pword.



Note: RSV indicates reserved bits that shall always be driven low.

Figure 9 - SKYchannel Address Pword

5.2.3 SKYchannel Address Information

The 44-bit SKYchannel address (ADD) is divided into two fields. The high 8 bits is the Board Select field, which shall specify the target board location. This allows up to 256 boards with a common address space in a single system. The low 36 bits are the on-board address field which shall specify the address local to the VME board. This provides 64 Gbytes of address space for local memory.

5.2.4 Packet Specific Code

The contents of the Packet Specific Code (PSC) field (bits 57:48) have different meanings for the read, write and interrupt packets.

- A basic read packet shall use bits [56:48] in conjunction with the source address to specify how many 16-bit words shall be read starting at the destination address (Pword 1 in the read packet). For a read packet, bit 57 shall be Reserved.
- A basic write packet shall clear bit 57 [57=0]. Bits [56:48] may be used to pass additional information between communicating modules.
- An interrupt packet shall set bit 57 [57=1]. The remaining bits in this field [56:48] should contain the interrupt mask bits which tell the destination board which processor to interrupt.
- A compare & switch packet should ignore all bits in the PSC field [57:48].

5.2.5 Routing Information

The 44-bit address Pword contains all the routing information for the SKYchannel Backplane. All switching and arbitration for ports occurs automatically in hardware to eliminate software overhead for setup and data routing.

5.2.6 CMS Bit

The Compare & Switch (CMS) bit shall be set [63=1] for compare & switch operations, otherwise cleared [63=0].

5.2.7 WRT Bit

The Write/Read (WRT) bit shall be set [64=1] for write operations, and cleared [64=0] for read operations.

5.2.8 RSP Bit

The Response (RSP) bit shall be set [65=1] in the address header of a write packet that is being returned to the requesting SKYchannel interface in response to a read packet. Otherwise RSP shall be cleared [65=0].

5.3 Data Pwords

The data Pword includes 64 bits for data and 8 bits for control purposes (Figure 10). The controllers on the interfaces use the control bits to determine:

- Byte enable for data types smaller than 64 bits.
- Address or data select.
- End of Packet.

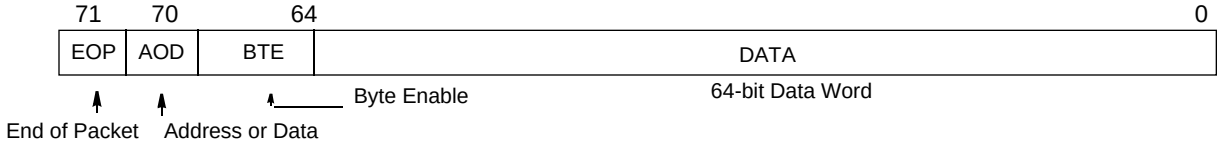


Figure 10 - SKYchannel Data Pword

5.3.1 End of Packet Field

The end of packet (EOP) bit shall be set [71=1] for the last data Pword in all packets. Otherwise, EOP shall be cleared [71=0]. Note that end of packet is indicated in the last Pword before the checkword.

5.3.2 Address/Data Field

The address or data (AOD) bit shall be cleared [70=0] in the address Pword.

5.3.3 Transfer Width and Alignment Specification

The SKYchannel data Pword shall contain a 6-bit Byte Enable field that indicates which bytes of the 64-bit data are valid as shown in Table 1. This enables data transfer widths of from one to eight bytes.

SKYchannel data words shall be 64-bit (8-byte) aligned. If the requested data either starts after the first byte and/or ends before the last byte, the appropriate bits shall be set in the Byte Enable (BTE) field according to Table 1. Note that the least significant 3 bits of address are ignored in all packets containing data Pwords (i.e. write packets). Those bits are included only as a convenience.

The BTE field is not intended for use in correcting endian issues. SKYchannel is a big-endian architecture. Little-endian devices connecting to SKYchannel shall convert to big-endian.

As an example of the use of the BTE field, consider a 64-bit data transfer that is aligned on a 32-bit boundary. The first data Pword would have a BTE = 011100, and the second data Pword would have a BTE = 010011.

Table 1 - Byte Enable Field Definition

Data Bits Description	69 BTE 64	63:56 B7	55:48 B6	47:40 B5	39:32 B4	31:24 B3	23:16 B2	15:8 B1	7:0 B0
No Valid Data	**0 0** 0 0 0 0								
BYTE 0	**0 0** 0 0 0 1								Valid
BYTE 1	**0 0** 0 0 1 0							Valid	
BYTE 2	**0 0** 0 1 0 0						Valid		
BYTE 3	**0 0** 1 0 0 0					Valid			
BYTE 4	**1 0** 0 0 0 1				Valid				
BYTE 5	**1 0** 0 0 1 0			Valid					
BYTE 6	**1 0** 0 1 0 0		Valid						
BYTE 7	**1 0** 1 0 0 0	Valid							
No Valid Data	**0 1** 0 0 0 0								
WORD 0	**0 1** 0 0 0 1							Valid	Valid
WORD 1	**0 1** 0 0 1 0					Valid	Valid		
WORD 2	**0 1** 0 1 0 0			Valid	Valid				
WORD 3	**0 1** 1 0 0 0	Valid	Valid						
LWRD 0	**0 1** 0 0 1 1					Valid	Valid	Valid	Valid
LWRD 1	**0 1** 0 1 1 0			Valid	Valid	Valid	Valid		
LWRD 2	**0 1** 1 1 0 0	Valid	Valid	Valid	Valid				
TWRD 0	**0 1** 0 1 1 1			Valid	Valid	Valid	Valid	Valid	Valid
TWRD 1	**0 1** 1 1 1 0	Valid	Valid	Valid	Valid	Valid	Valid		
QWRD 0	**0 1** 1 1 1 1	Valid	Valid	Valid	Valid	Valid	Valid	Valid	Valid
Memory Parity or Uncorrectable Error	**1 1** 0 0 0 1								

5.4 Arbitration

The SKYchannel packet bus arbitration is implementation dependent. For example, one implementation uses a round-robin arbitration scheme. Round-robin arbitration assigns the lowest priority to the port that last used the packet bus. Other arbitration schemes are possible.

5.5 Error Handling

During packet transmission, some conditions may occur that generate a hardware interrupt to indicate that an error has occurred. The SKYchannel Backplane shall route all such interrupts to the SKYchannel Backplane Controller (BC) board (the lowest-numbered board attached to a SKYchannel Backplane) over the INT/CONFIG signal (described in Table 4). See Section 7 for a timing diagram showing the interrupt sequence. The BC should notify the application that an error has occurred.

5.5.1 SKYchannel Backplane Error Detection

The SKYchannel Backplane shall provide interrupt signals for the following errors:

1. Port connection error, e.g., destination port does not exist.
2. A port's FIFO ready signal is deasserted for an implementation-defined number of microseconds.
3. An EOP does not occur within an implementation-defined number of microseconds after connection has been established; this is also known as a jabber time-out.
4. A packet was sent from a master interface to a port that does not have a slave interface
5. A packet was sent from a slave interface to a port that does not have a master interface.

5.5.2 P2 Interface Checkword

The transmitting SKYchannel P2 Interface shall append a 72-bit checkword Pword the EOP cycle of a data transfer. The checkword shall consist of 72 parity bits, each one representing the parity of all the valid bits transmitted in that bit position for that packet. This may be thought of as parity on 72 columns of data and control. Adjacent columns, e.g., Gbus[2] and Gbus[1], shall generate parity of opposite polarity—even columns producing even parity, odd columns odd parity. Even parity implies that the number of valid ones in a transmitted column plus the corresponding column parity bit is an even number. Odd parity implies an odd number of ones including the parity bit in a column.

The receiving SKYchannel P2 Interface similarly should generate parity on the received data columns and compares its checkword with that appended by the transmitting port. If the packet is to be forwarded within the VME board, the checkword should be stripped after checking and not be part of forwarded packet. If the checkwords do not match, the P2 interface should indicate an local hardware error. The receiving SKYchannel P2 Interface may send an interrupt packet to the SKYchannel Backplane Controller to indicate the error.

5.5.3 Data Pword Error Handling

Modules connected to SKYchannel may have error detection as part of their circuitry. Data Pwords in which an uncorrectable error exists shall indicate the error condition to the SKYchannel destination. Such a condition shall be encoded in the BTE field of the data Pword (bits [69:64]) as shown in Table 2.

Table 2 - BTE Field of Data Pword Error Condition

BTE						Description
69	68	67	66	65	64	
1	1	0	0	0	1	Uncorrectable Error

6 Physical Layer Specification

This section describes how the SKYchannel operates with the P2 Interface and SKYchannel Backplane to provide 320 MB/sec performance throughout a VME system as diagrammed in Figure 11.

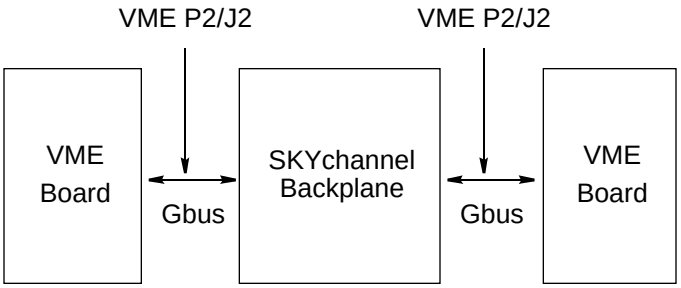
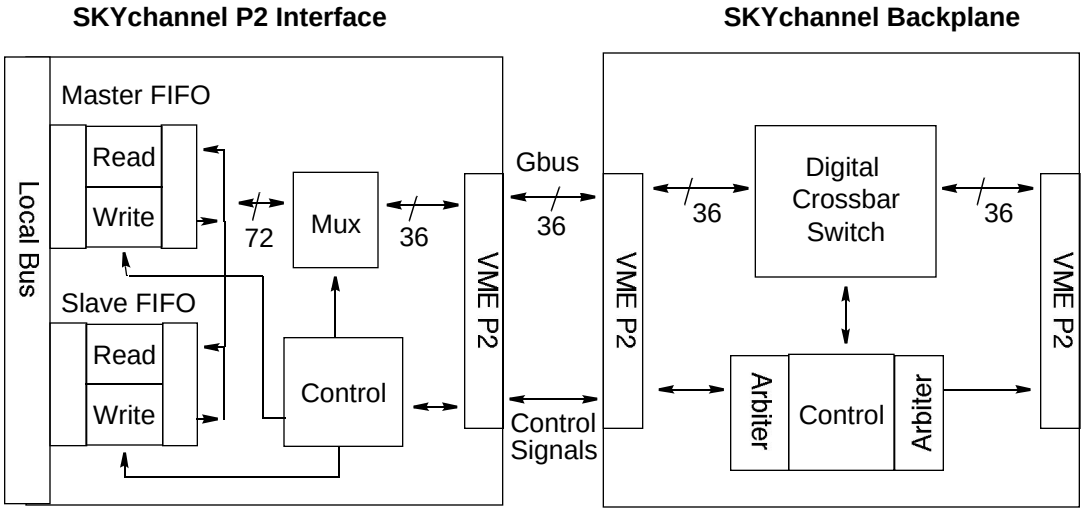


Figure 11 - SKYchannel Packet Bus in a VME System

6.1 SKYchannel P2 Interface

The SKYchannel P2 Interface is the circuitry on a VMEbus board that communicates with the SKYchannel Backplane through the VME P2/J2 connectors. The SKYchannel P2 Interface connects to the SKYchannel Backplane via a Mux/Demux chip and a set of Master/Slave FIFOs. Figure 12 is a diagram of the interface components for the SKYchannel P2 Interface and the SKYchannel Backplane.



*Note: Only two ports shown. The digital crossbar switch is not required in a bus implementation.

Figure 12 - SKYchannel P2 Interface and SKYchannel Backplane

6.1.1 Standard Register Set

All SKYchannel P2 Interface implementations shall have three 8-bit standard registers (Figure 6). These registers shall be loaded with configuration information sent serially over the INT/CONFIG signal by the SKYchannel Backplane after reset. The registers shall be filled by toggling the INT/CONFIG signal, with each clock tick filling one bit. (See section 7 for a waveform diagram covering this operation.) Although the SKYchannel Backplane shall send exactly 64 bits of configuration information, only the first 24 bits is needed for the three required registers. The remaining 40 bits of the configuration sequences are Reserved, and the SKYchannel P2 Interface shall not consider the configuration complete until it has received them. The SKYchannel P2 Interface may load those remaining 40 bits into an additional five registers.

The first register shall be loaded with the board number from 0 to 255. After reset, the SKYchannel Backplane arbiter shall serially fill the board register with an 8-bit value which identifies the board position. The second register shall provide two functions: identifying the SKYchannel Board Controller (BC), and providing configuration status. Bit 0 shall identify the board designated as the BC. The BC shall always be the lowest-numbered board in the system (bit 0 = 1). Bit 1 indicates the configuration status. This bit is initially set to 0 after reset. The SKYchannel P2 Interface shall set bit 1 to 1 after the registers have been programmed. The third register shall identify the SKYchannel VITA specification revision number. A value of 0 shall indicate ANSI/VITA 10-1995

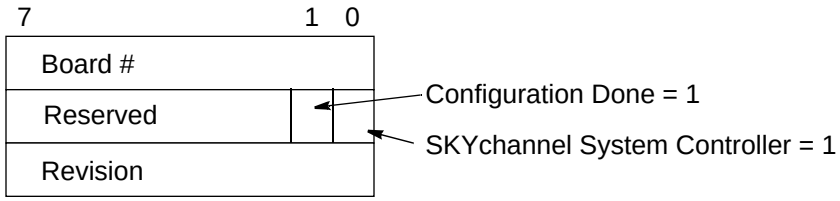


Figure 13 - SKYchannel P2 Interface Registers

6.1.2 P2 Interface FIFOs

The SKYchannel P2 Interface connects to the on-board SKYchannel through a pair of decoupling, bidirectional FIFOs, one for Master reads/writes and one for Slave reads/writes. Note that both Master and Slave FIFOs are required when the device is both a Master and a Slave. A Slave-only or Master-only device requires a single bidirectional FIFO. The FIFO shall have the ability to operate independently from the P2 Interface bus. The FIFO shall support data rates up to 40 MHz. The bidirectional FIFO implementation shall have two separately clocked FIFOs that are able to buffer data in opposite directions. Each unidirectional portion of the FIFO shall have the ability to read data from its array in the same order it is written. Each unidirectional portion of the FIFO shall be 72 bits wide and be deep enough to hold a minimum of two SKYchannel packets of the maximum size. Transfers through the interface shall be gated to a continuous clock by enable signals. As an example, one implementation uses four 18-bit wide Texas Instrument FIFOs (SN74ABT7819) for each decoupling, bidirectional FIFO.

The FIFOs shall be referenced from their interface to the local bus. The Master FIFO shall be responsible for sending write, read, compare & switch and interrupt packets to Slave FIFOs. The Slave FIFO shall be responsible for sending response packets in reply to the Master. The SKYchannel P2 Interface shall always send Slave FIFO response packets to the SKYchannel Backplane before the Master FIFO packets. The table below lists the specific roles for each FIFO.

Table 3 - SKYchannel Master/Slave FIFOs; Packets Sent and Received

FIFO	Packet Type Sent	Packet Type Received
Master	Write Packets Read Packets Compare & Switch Packets Interrupt Packet	Response Packets
Slave	Response Packets	Write Packets Read Packets Compare & Switch Packets Interrupt Packet

All FIFO memories are referred to by their local bus function. Thus, the local bus to P2 Interface memory of the FIFO, which is used for Writes, is called the Write FIFO and conversely the FIFO used for reads is called the Read FIFO. This is illustrated in Figure 14.

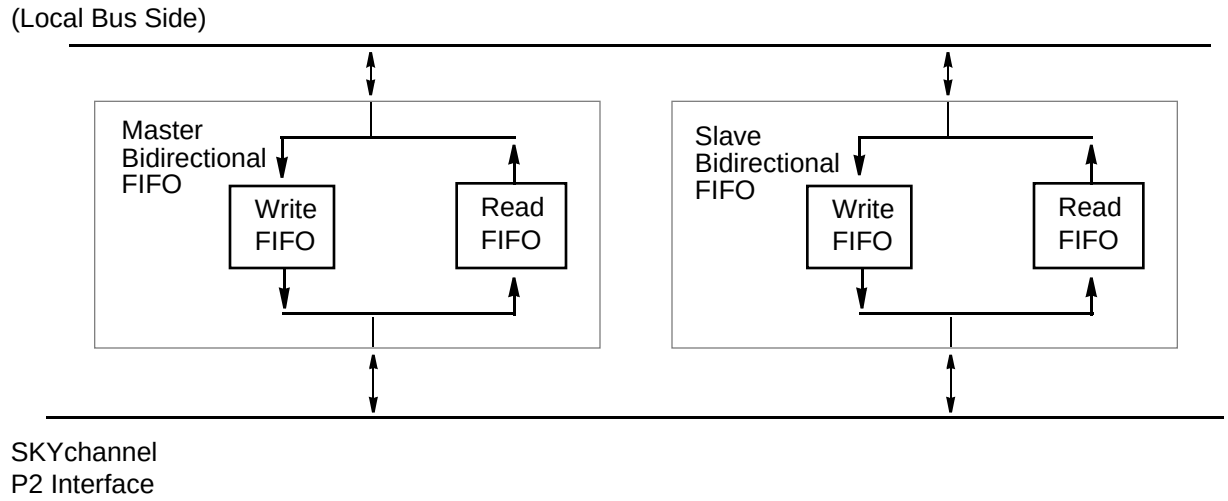


Figure 14 - SKYchannel P2 Interface Master/Slave FIFOs

The Local Bus side shall be exclusively controlled by the local bus control logic and is function-block dependent. The P2 Interface side is exclusively controlled by the logic which interfaces to the SKYchannel arbiter. Once one side writes into the FIFO, the other side shall be responsible for reading it.

6.1.3 SKYchannel P2 Interface Arbitration Signals

The P2 Interface shall use three arbitration signals when arbitrating for the bus. These signals are Packet Available (PA_), Chip Select (CS_) and Read Enable (REN) as defined in Table 4. All SKYchannel P2 interfaces shall be able to support the full clock range between 20 to 40 MHz without hardware modification.

6.1.4 P2 Interface Signals to SKYchannel Backplane

Table 4 describes the signals that shall be transferred between the SKYchannel P2 Interface and the SKYchannel Backplane. Except for VCC & GND, each port shall have its own set of control signals.

Table 4 - SKYchannel P2 Interface Signals for Backplane Implementation

Mnemonic	Description
CLK	20 to 40 MHz reference clock. Input to the P2 interface. Data on the Gbus is clocked at 2x this rate.
Gbus <35:0>	Bidirectional Bus. The 36-bit Gbus carries the 72-bit wide SKYchannel packets. SKYchannel bits [71:36] are transferred first followed by bits [35:0]. Transfers takes place at a 40 to 80 MHz clock rate.
PA_	Packet Available. Output from the P2 interface. Asserted active low by the P2 Interface when one or more packets are available. Deasserted when there are no additional packets to transfer. This signal can only be deasserted when CS_ and REN have both been asserted indicating that the packet has been granted. Once PA_ is asserted it must not be removed until at least one packet has been transferred.
MFR	Master FIFO Ready. Output from the P2 interface. Asserted active high by the P2 Interface when its Master read FIFO is ready to accept packets from the SKYchannel Backplane. This signal shall be asserted low if there is not enough room left in the FIFO to assure the receipt of a full size packet (131 Pwords).
SFR	Slave FIFO Ready. Output from the P2 interface. Asserted active high by the P2 Interface when its Slave read FIFO is ready to accept packets from the SKYchannel Backplane. This signal shall be asserted low if there is not enough room left in the FIFO to assure the receipt of a full size packet (131 Pwords).
REN	Read Enable. Input to the P2 interface. Asserted active high by the SKYchannel Backplane arbiter during packet transfers from the initiating P2 interface to the SKYchannel Backplane. This signal causes the interface to shift the next data word. This signal also indicates that the P2 interface has been granted use of the connection.
WEN	Write Enable. Input to the P2 interface. Asserted active high by the SKYchannel Backplane arbiter during packet transfers from the SKYchannel to the P2 Interface. This signal is asserted to shift data into the destination P2 FIFO. This signal is the only indication given to the destination P2 that the interface is receiving data. If the interface has its FIFO ready signals asserted it must be prepared to clock data when this signal is asserted.
CS_	Chip Select. Input to the P2 interface. Asserted active low by the SKYchannel Backplane to indicate to the P2 interface that it must drive its header to the Gbus. The header must be driven to the Gbus immediately so that the SKYchannel arbiter can determine the packet destination. CS_ shall remain asserted throughout the entire transfer.

Table 4 - SKYchannel P2 Interface Signals for Backplane Implementation

Mnemonic	Description
DATVAL_	Data Valid. Output from the P2 interface. Asserted active low by the initiating P2 Interface during valid data transfers. It must be deasserted one cycle before data becomes invalid on the Gbus. When this signal is driven to the SKYchannel by the source P2, the SKYchannel arbiter shall remove REN and WEN one clock cycle later. CS_ shall remain asserted, maintaining the connection through the SKYchannel backplane. The data transfer shall resume one clock cycle after DATVAL_ is asserted. DATVAL_ shall not be held deasserted for long periods of time for performance reasons. The DATVAL_ of a specific P2 interface is examined by the arbiter both during arbitration to check the header and during the time that interface is transferring data.
RESET_	Reset. Output from the P2 interface (SKYchannel Backplane Controller only). Asserted active low. This signal resets the SKYchannel Backplane. No other P2 Interface connected to the same SKYchannel Backplane drives or receives this signal.
INT/ CONFIG	Interrupt/Configuration. This is a bi-directional signal. After a system reset the SKYchannel Backplane uses this signal to serially configure the P2 interfaces. After configuration has completed, this line is used by the SKYchannel Backplane to indicate an error interrupt to the SKYchannel Backplane Controller. The P2 interface at the Backplane Controller board location shall be the only interface that can be interrupted by this line. There shall be a board at that location that is capable of properly processing an error interrupt. After the interrupt information is received, the P2 interface asserts this line to acknowledge the interrupt, and deasserts it to indicate that the interrupt was handled.
VCC	Power. +5V.
GND	Power. Ground.

6.1.5 Packet Transfers and the P2 Interface

When the SKYchannel P2 Interface detects data in its FIFO, it shall generate a PA_ signal to the SKYchannel. PA_ may be asserted before the packet has finished loading into the FIFO. The arbiter shall detect the PA_ and, if it is not busy, it shall assert CS_ on the next clock cycle. Upon detecting the CS_ signal, the P2 interface shall enable its GBUS drivers and drive the high 36 bits of the header onto the bus.

The header shall be driven to the bus during the clock cycle in which CS_ is asserted. The arbiter shall then examine the Board Select field of the address header bits [43:36] (Gbus bits 7:0). At this point, PA_ shall be qualified with DATVAL_. This allows for reordering prioritized packets or other instances when the header may become invalid. If the board position selected is populated, the arbiter shall examine the FIFO Ready lines of the target interface to determine the interface's readiness to receive a new packet. If the Response bit [65] (Gbus bit 29) is set in the packet header, the packet is intended for the master FIFO set so the MFR signal shall be checked. If the Response bit is not set, the packet is intended for the slave FIFO set and the SFR signal shall be checked. In order for the FIFO to receive this new packet, the appropriate FIFO Ready signal must be asserted. If the signal is not asserted, the arbiter shall not grant the connection and should try again later. If the FIFO Ready signal indicates that the FIFO can accept a new packet then

the appropriate REN and WEN signals shall be asserted establishing the connection. This can be asserted in as little as one clock cycle after CS_.

At this point a connection has been established and one half of a Pword shall transfer between the two FIFOs on each edge of the Gbus clock cycle (CLK) as long as REN and WEN are asserted. The data on the GBUS shall alternate between the high and the low 36 bits of the Pword. The REN and the WEN shall remain asserted until DATVAL_ becomes deasserted or EOP is encountered. If DATVAL_ is deasserted by the source interface, it indicates that the source FIFO does not currently contain valid data, and REN and WEN shall be deasserted one clock cycle later, halting the data transfer between the FIFOs. The data transfer shall resume one clock cycle after the interface reasserts DATVAL_. The connection shall remain open until EOP is encountered in the data stream. At that point, the checkword shall be transferred at which time CS_, REN, and WEN shall be deasserted closing the connection. The arbiter is now free to grant a new connection.

The PA_ signal shall be de-asserted by the requesting interface before the arbiter completes the transfer of the packet unless there are additional packets to be transferred. PA_ does not have to toggle if there are additional packet requests; however, if there are no new packets and the PA_ signal is not removed before the arbiter returns to its arbitration state then an erroneous grant can be generated. The PA_ signal shall not be deasserted until the first REN. The REN signal is the indication that the packet request has been granted. The time required to connect to an available path (without contention) from the time that PA_ is asserted by the P2 interface is as follows:

Table 5 - Clock Cycles Required for Path Connection

Event	Number of clock cycles
PA_ to CS_	1
Header Decode	1
Header Transfer (REN/WEN)	1
Data Transfer (REN/WEN)	1 per packet word
Checkword (REN/WEN)	1
Total Clock Cycles	5

Table 5 assumes a 40 MHz clock and describes a typical connection in which 2 clock cycles (which is equivalent to 50ns) are required to make a connection. One additional cycle is needed to transfer the header; thus, it requires 75ns to start the data transfer. A minimum-sized 3-Pword packet should transfer in a total of 5 cycles including the checkword for a total of 125ns. The arbiter should remove CS_, REN, and WEN on the same cycle that the checkword is transferred. Removing these signals shall turn off the source interface's bus drivers and allow the bus to return to the high impedance state. The earliest the CS_ can be reasserted is one clock cycle later; for this reason, a bus recovery wait state is built into the PA_ arbitration cycle and an additional state is not required. The full bus cycle time for a minimum 3-Pword packet is 5 cycles (125 ns), and for a maximum 131 Pword packet is 133 cycles (3.325 µsecs). Latency is considered to be the amount of time required to begin the transfer of actual data. The SKYchannel latency number is 75 ns.

When the local bus starts to load its end of the FIFO, the PA_ signal may be asserted. If the interface is a slow master it should wait until the entire packet is in the FIFO before asserting PA_. This decouples the

speed of the local interface from the high-speed SKYchannel. However, slave-generated response packets shall always assert PA_ before the entire packet is built to lower the read latency. The CS_ signal can be asserted one clock cycle after PA_ is presented; therefore, a valid header word shall be available at the GBUS output registers at a minimum of one clock cycle after PA_ is asserted.

6.1.6 Resetting the SKYchannel P2 Interface

Each SKYchannel-enabled VME board shall reset its SKYchannel P2 Interface upon receiving the VME_SYSRST. If that board is the SKYchannel Backplane Controller, it shall also reset the SKYchannel Backplane by asserting RESET_ for the same number of clock cycles as VME_SYSRST. The deassertion of this signal is the signal for the SKYchannel Backplane to begin the configuration sequence.

If a SKYchannel-enabled VME board is capable of a local hardware reset, during that local reset it should reset all portions of the SKYchannel P2 Interface except for the Standard Configuration Registers loaded by the SKYchannel Backplane as defined in section 6.1.1.

6.2 SKYchannel Backplane

The SKYchannel Backplane is the circuitry that connects the SKYchannel P2 Interfaces on multiple VME boards to facilitate interboard communication. Typically, this is implemented as an overlay backplane attached to rear of VME J2. However, other physical implementations are possible, and the functionality may even be implemented by a set of physical pieces to make one virtual backplane.

The SKYchannel Backplane consists of three functional blocks. The first block contains the SKYchannel data path. The second functional block is the SKYchannel Backplane arbiter which controls and monitors access to the SKYchannel Backplane from all ports. This block also monitors the SKYchannel Backplane for connection time-outs. The third functional block is the clock generator.

6.2.1 SKYchannel Backplane Data Path

The SKYchannel Backplane data path for each port shall be 36 bits wide. Data words from the P2 Interface FIFO shall be clocked into the P2 TTL transceiver registers in two parts; first the upper Pword, then the lower Pword. Although the Gbus is half the width of a Pword, it maintains the high throughput with a clock rate that is double that of the reference CLK signal. The data path may be implemented as a bus for a high-performance, lower cost implementation, or it may be implemented as a digital crosspoint switch for multiple channels. Bussed implementations of the SKYchannel Backplane are typically limited to 6 VME slots for full speed performance using current technology.

6.2.2 SKYchannel Backplane Arbiter

The SKYchannel Backplane arbiter controls and monitors access to the SKYchannel Backplane from all SKYchannel P2 ports. Requesting ports arbitrate via a three-wire interface per port: PA_, CS_ and REN. The destination port uses the SFR and MFR signals to indicate whether a connection can be made. The arbiter also drives WEN to the destination port to indicate that the connection has been made.

6.2.3 SKYchannel Backplane Clock Generation

The SKYchannel Backplane shall generate and distribute a 20 to 40 MHz reference (CLK) to the SKYchannel P2 Interface ports. All P2 interfaces shall be able to adjust to a clock in this range during the power-up sequence. The P2 interface should synchronize to the reference clock using phase lock loops (PLL). This keeps the clock skew and loading to a minimum. The skew on the PLLs should be kept to

700 ps. The P2 interface should then regenerate the CLK signal and a double speed clock (2XCLK) signal from the PLL. The 2XCLK should then be used to clock the 36-bits in parallel through the data path.

The provision for operation at a reduced rate provides trade-offs of physical medium, distance, and cost. Although intended as a build option, the clock rate may be changed in the field while the system is powered down, and all SKYchannel P2 interfaces shall be capable of adjusting to the new clock.

6.2.4 SKYchannel Backplane Power

The power for a SKYchannel Backplane is provided by the VCC pins in the B rows of all the slots to which the SKYchannel Backplane is attached. For example, a SKYchannel Backplane covering 8 slots would draw current from 16 VCC pins. The maximum current drawn by the SKYchannel Backplane shall observe the requirements set forth in ANSI/VITA 1-1994. Note that current drawn through the pin in the rear of the VME backplane does not subtract from the allotment for current drawn from the front of the backplane.

6.3 P2 Pinout

The SKYchannel Backplane uses rows A and C of the P2 connector plus four pins in Row B (2 Gnd, 2 +5V) for a total of 68 pins.The VME tail pins shall be.521” (13 mm) long with gold-plated tails. The SKYchannel Backplane and the SKYchannel P2 Interface shall pinout the signals as shown in Table 6.

Table 6 - P2 Pinouts for SKYchannel on VME P2/J2

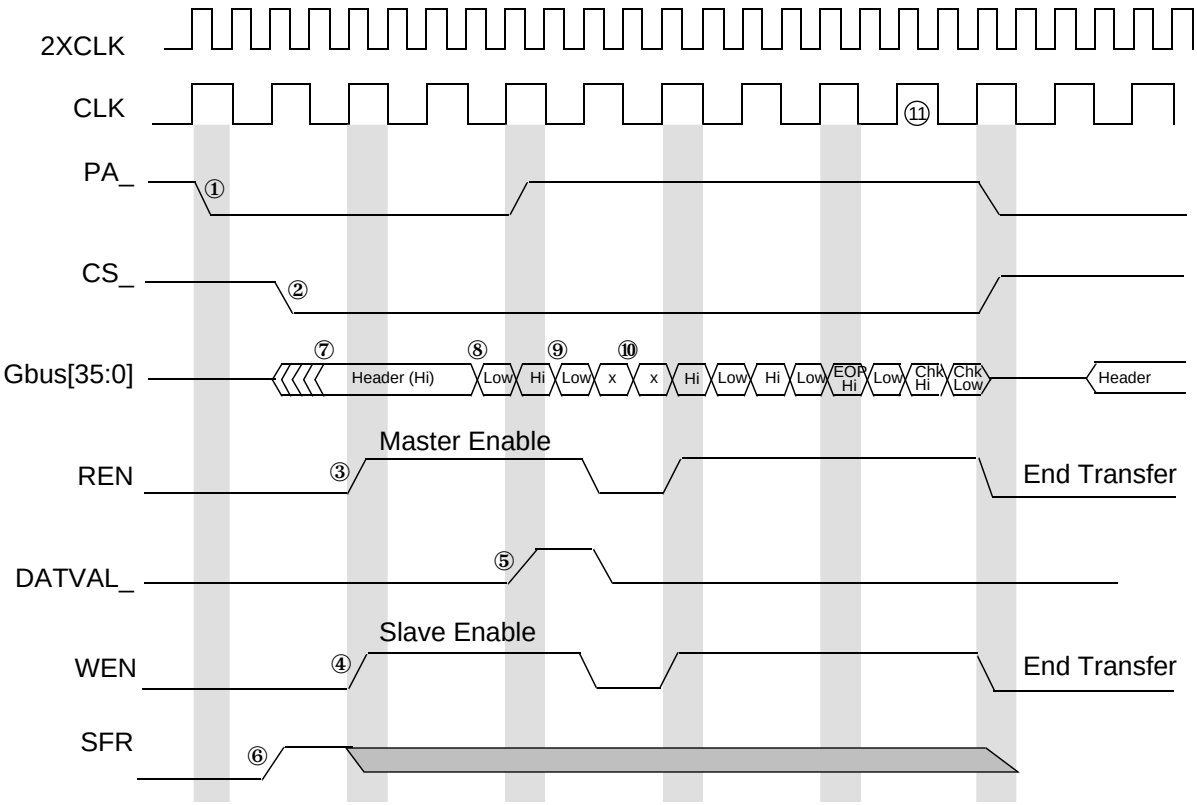
Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	B1	VCC	C1	GND
A2	GB<0>	B2	GND	C2	GB<1>
A3	GB<2>	B3	N.C.	C3	GB<3>
A4	GB<4>	B4	N.C.	C4	GB<5>
A5	GB<6>	B5	N.C.	C5	GB<7>
A6	GB<8>	B6	N.C.	C6	GB<9>
A7	GND	B7	N.C.	C7	GND
A8	GB<10>	B8	N.C.	C8	GB<11>
A9	GB<12>	B9	N.C.	C9	GB<13>
A10	GB<14>	B10	N.C.	C10	GB<15>
A11	GB<16>	B11	N.C.	C11	GB<17>
A12	GB<18>	B12	N.C.	C12	GB<19>
A13	GND	B13	N.C.	C13	GND
A14	GB<20>	B14	N.C.	C14	GB<21>
A15	GB<22>	B15	N.C.	C15	GB<23>
A16	GB<24>	B16	N.C.	C16	GB<25>
A17	GB<26>	B17	N.C.	C17	GB<27>
A18	GB<28>	B18	N.C.	C18	GB<29>
A19	GND	B19	N.C.	C19	GND
A20	GB<30>	B20	N.C.	C20	GB<31>
A21	GB<32>	B21	N.C.	C21	GB<33>
A22	GB<34>	B22	N.C.	C22	GB<35>
A23	GND	B23	N.C.	C23	GND
A24	DATVAL_	B24	N.C.	C24	PA_
A25	GND	B25	N.C.	C25	GND
A26	WEN	B26	N.C.	C26	SFR
A27	GND	B27	N.C.	C27	GND
A28	REN	B28	N.C.	C28	MFR
A29	GND	B29	N.C.	C29	GND
A30	CS_	B30	N.C.	C30	RESET
A31	GND	B31	GND	C31	INT/CONFIG
A32	CLK	B32	VCC	C32	GND

7 Waveform Diagrams

Waveform diagrams are provided for a successful packet connection, a packet connection that has been denied due to a FIFO not ready condition, a connection that waits until Master FIFO Ready is asserted, a reset and configuration sequence, and an interrupt.

7.1 Packet Available, P2 Interface Granted Bus

The packet available (PA_) signal shall asserted by the P2 interface when the FIFO has data available. The SKYchannel Backplane arbiter shall respond with CS_ when it is ready to examine the packet header. The arbiter decodes the address header bits [43:36] (Gbus [7:0]) to determine the transfer destination and various other bits to determine the type of transfer. The arbiter then checks the FIFO ready signals of the destination interface. If the response bit is set, Master FIFO Ready (MFR) is checked; if the response bit is not set Slave FIFO Ready (SFR) is checked. The arbiter then asserts REN and WEN which enable a transfer on each clock cycle as long as the Data Valid (DATVAL_) signal remains low. If the DATVAL_ shall toggle, the arbiter permits transfer of one high/low data word before suspending the transfer. The transfer resumes one clock cycle after DATVAL_ is asserted. Detection of the end of packet (EOP) de-asserts REN, WEN, and CS_ after the checkword has been transferred.



Note: All signals except GBUS[35:0] are referenced to CLK.
GBUS[35:0] are clocked at twice that rate.

Figure 15 - Packet Available, P2 Interface Granted Bus

Note: Numbers in Figure 15 refer to the timings given in Table 8.

7.2 Packet Available, P2 Interface Not Granted Bus (Slave FIFO Not Ready)

The PA_ signal shall be asserted by the P2 interface when the FIFO has data available. The SKYchannel Backplane arbiter shall respond by asserting the chip select (CS_) signal which causes the address header to be loaded onto the bus. The SKYchannel Backplane arbiter shall decode the header and examine the destination FIFO Ready signal. If the FIFO is not ready (SFR does not assert) then the arbiter shall remove CS_. At this point the connection has failed. The arbiter shall then attempt to connect one P2 interface with a response packet. At the end of the attempt, or the transfer if a response packet was available, the arbiter shall return to the failed P2 interface and retry to establish the connection. This sequence shall continue until the connection is established.

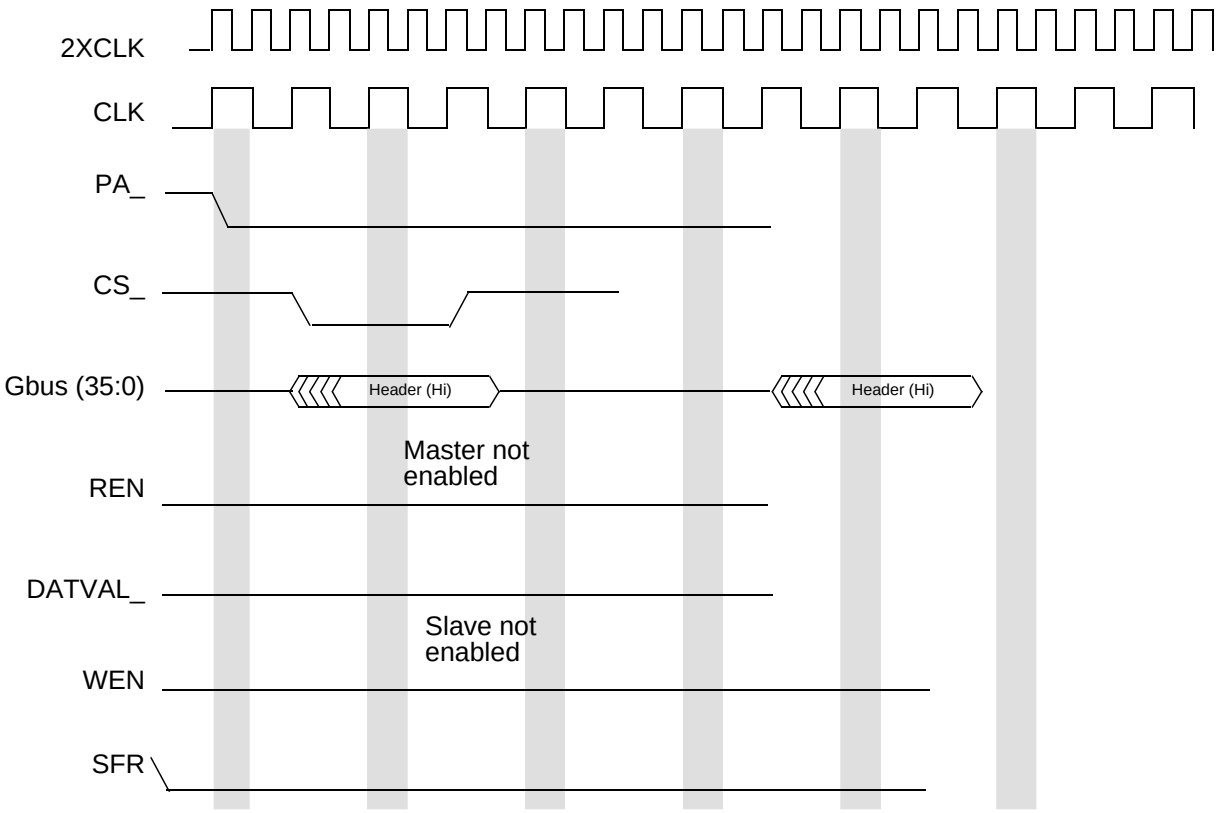


Figure 16 - Packet Available, P2 Interface Not Granted Bus

7.3 Packet Available, P2 Interface Not Granted Bus (Master FIFO Not Ready)

The PA_ signal is asserted by the P2 interface when the FIFO has data available (a). The SKYchannel arbiter responds by asserting the chip select (CS_) signal (b) which causes the address header to be loaded onto the Gbus (c). DATVAL is asserted throughout the transaction, since the data lines contain valid data. The header is decoded; the Response bit is set (d; shown as the RESP bit in the Arbiter), so the destination Master FIFO Ready signal is examined. Because the Master FIFO is not ready (e) then the arbiter shall removes CS_ (f) and deasserts the Gbus lines. However, PA_ is still asserted, so CS_ shall be asserted again (g). This time, MFR is asserted, so the WEN and REN lines shall be asserted (h) and the transfer shall proceed until EOP is sensed (not shown in diagram).

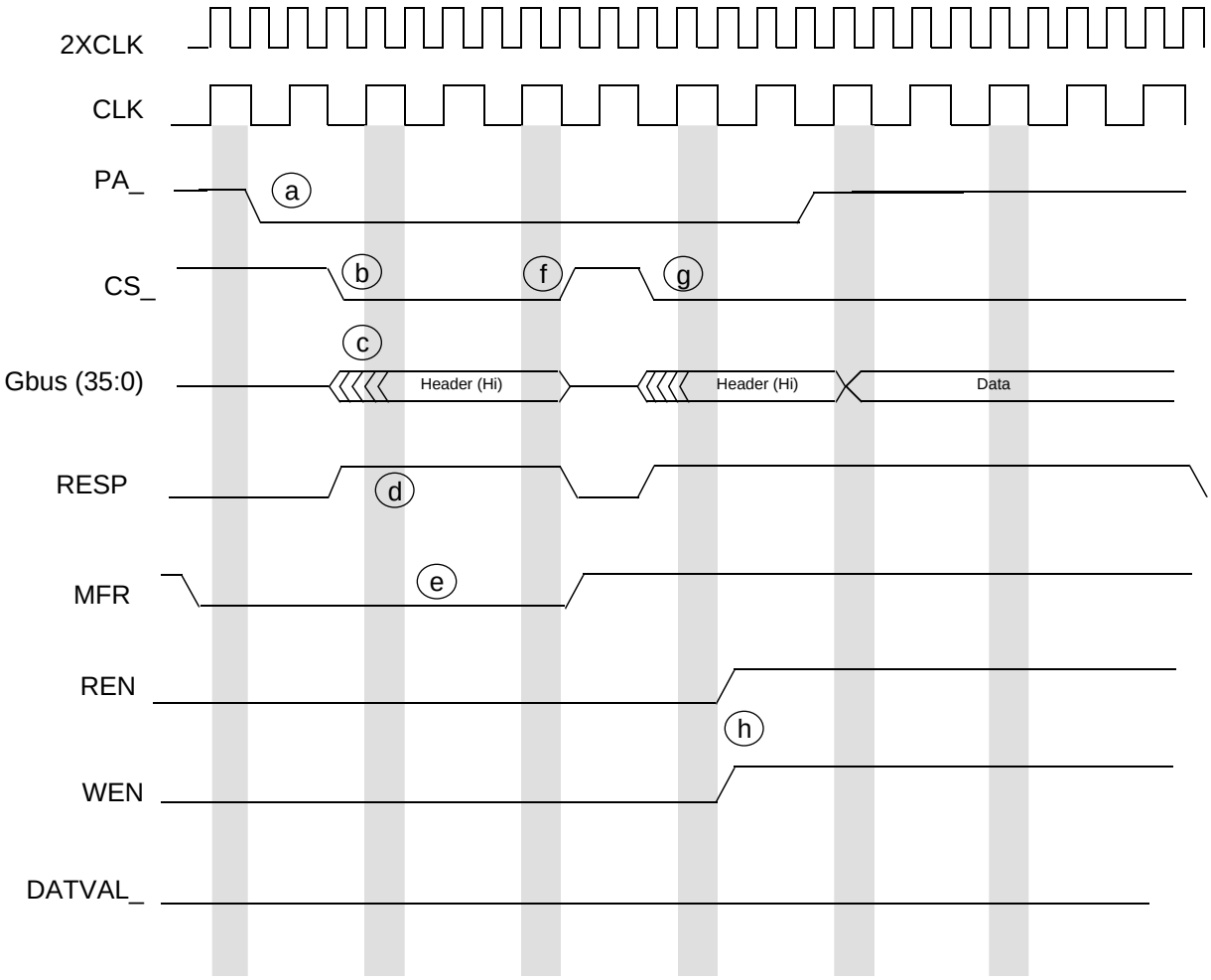


Figure 17 - Packet Available, Master FIFO Not ready

7.4 Configuration Sequence

The SKYchannel Backplane shall use the INT/CONFIG signals to load configuration registers on each SKYchannel board. After RESET is deasserted, the Serial Loader on the SKYchannel Backplane shall hold the INT/CONFIG line to each board high for 6 to 10 clocks, then drive it low for one clock (a). This one-clock high-to-low transition is the Preamble. Following the Preamble bit, the Serial Loader shall drive the register bits over the INT/CONFIG line to each SKYchannel board connected to the SKYchannel Backplane. The first 24 bits load the three standard SKYchannel registers; the subsequent 40 bits are don't-care (b). After the last register bit, the Serial Loader shall hold the INT/CONFIG lines low for one clock to indicate configuration completed (c), then releases the lines. After receiving this "configuration completed" bit, the SKYchannel P2 Interface on each board shall set the Configuration Done bit (bit 1) in the second of the three SKYchannel standard registers (not shown in diagram).

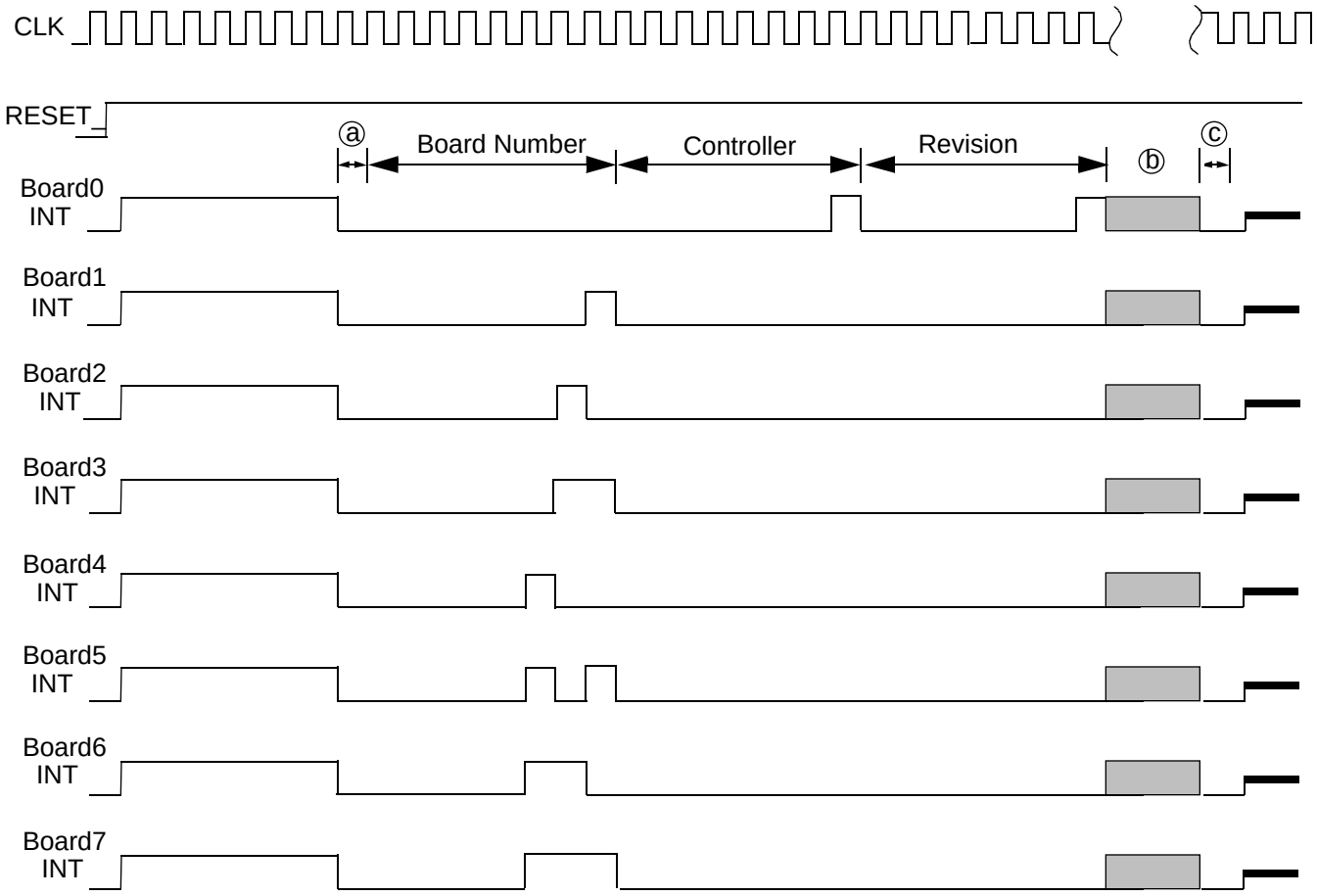


Figure 18 -Configuration Sequence, Eight Boards

7.5 Interrupt Sequence

The SKYchannel Backplane shall use the INT/CONFIG signal to send interrupts to the SKYchannel Backplane Controller (BC) board 0 (INT0 in the diagram below). After the configuration sequence has completed, the SKYchannel Backplane shall tristate the INT/CONFIG line. When an error condition is detected by the SKYchannel Backplane, it shall drive INT/CONFIG low for one to seven clocks and then high for one clock (a). [The Backplane in the example below writes eight bits—7 low, then one high]. Following this Interrupt Alert bit, the Backplane may transmit a serial data stream of up to 40 bits to the SKYchannel Controller board. The P2 Interface on the SKYchannel Backplane Controller may load this serial stream into five 8-bit registers. The diagram below shows five 8-bit registers being written, 40 bits in all (b). On the next clock, the Backplane shall drive the INT/CONFIG line to the BC high for one clock (c), then releases the line. After receiving the interrupt data and handling the interrupt, the BC shall drive the INT line high for one clock as an interrupt acknowledge (not shown in the diagram) and then release the line. At this point, the BC may start the sequence over to send the next interrupt.

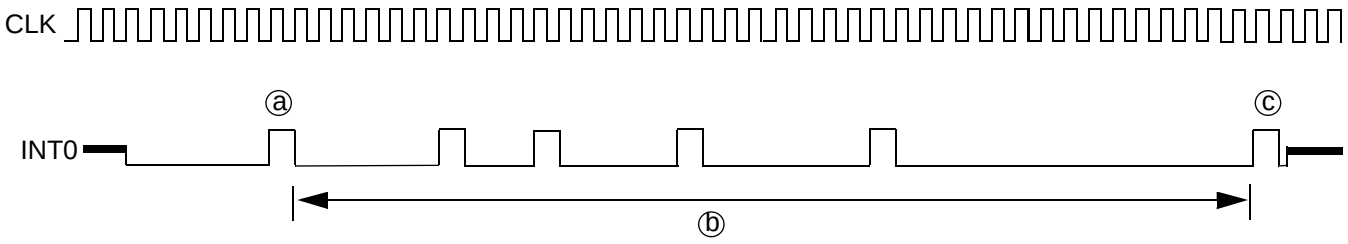


Figure 19 - Interrupt Sequence, Backplane to SKYchannel Controller

7.6 P2 Interface Electrical Characteristics of SKYchannel Signals

The Electrical characteristics of the SKYchannel signals are listed in Table 8. All bus signals are TTL.

Table 7 - Signal Line Summary; Electrical Characteristics

Signal Mnemonic	Signal Name	Driver Type/Direction	Recommended Terminator
CLK	20 to 40 MHz Ref Clock	Totem Pole, Input to P2	25 Ω series res at source
DATVAL_	Data Valid	Totem Pole, Output from P2	25 Ω series res at source
MFR	Master FIFO Ready	Totem Pole, Output from P2	25 Ω series res at source
SFR	Slave FIFO Ready	Totem Pole, Output from P2	25 Ω series res at source
INT/CONFIG	Interrupt Request	Bidirectional, Input to P2	25 Ω series res at source
PA_	Packet Available	Totem Pole, Output from P2	25 Ω series res at source
REN_	Read Enable	Totem Pole, Input to P2	25 Ω series res at source
WEN_	Write Enable	Totem Pole, Input to P2	25 Ω series res at source
CS_	Chip Select	Totem Pole, Input to P2	25 Ω series res at source
RESET	Reset	Totem Pole, Input to P2	25 Ω series res at source

7.7 P2 Interface Timing Parameters of SKYchannel Signals

The Timing parameters for the SKYchannel signals are listed in Table 8 (numbers refer to Figure 15). All times are in nanoseconds (ns) and are measured on the rising (falling) edge for signals that are asserted active high (low). Unless otherwise noted, all times are propagation delays. All SKYchannel P2 Interfaces and SKYchannel backplanes shall meet these timing parameters over the full range of temperature and voltage levels for which those products are specified.

Table 8 - Signal Timing Parameters

Reference Number	Description	Min	Max
1	CLK to PA_	0	10
2	CLK to CS_	0	5
3	CLK to REN	0	5
4	CLK to WEN	0	5
5	CLK to DATVAL_	0	10
6	CLK to SFR	0	10
7	CS_ to GBUS	0	6
8	CLK (either edge) to GBUS	0	6
9	GBUS to CLK (either edge) Setup	3	—
10	GBUS to CLK (either edge) Hold	0	—
11	CLK duty cycle	40%	60%